IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER (Large Entity)

Application Number: **09/966,095**

Group Art Unit: **2111**

Filed: **October 1, 2001**

Examiner Name: **Dang, Khanh**

Applicant: **Balay**

Attorney Docket Number: **Balay 2-1**

TITLE: **PCI/LVDS HALF BRIDGE**

Total Number of Pages in this Submission: **14**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

Transmitted herewith is:
An Appeal Brief (17 Pages) (In triplicate)

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Respectfully submitted,

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Date: October 27, 2005

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Our Ref.: **20-143**

In re Patent Application of:
BALAY et al.
Title: **PCI/LVDS HALF BRIDGE**

October 27, 2005

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Applicants submit herewith the following Appeal Brief in triplicate as required by 37 C.F.R. § 1.192.

(1) REAL PARTY IN INTEREST

The real party in interest is Agere Systems Inc.

(2) RELATED APPEALS AND INTERFERENCES

The Applicants and their legal representatives and assignee are not aware of any other appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in the appending appeal.

(3) STATUS OF THE CLAIMS

Claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 are pending in this application. Claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 stand rejected.

(4) STATUS OF ANY AMENDMENT FILED SUBSEQUENT TO FINAL REJECTION

No Amendment has been filed subsequent to the Final Rejection issued by the Examiner on June 2, 2005.

(5) SUMMARY OF THE INVENTION

A system and method are providing that allows for communications between two computer bus segments. Two half-bridge circuits are connected to respective computer bus segments and frame data for a high speed transfer of the data between the half-bridge circuits. A common application is to connect multiple PCI segments that are individually limited to the number of components connected thereto. Connection through the high speed half-bridge circuits allows additional PCI components to communicate on a second computer bus segment, acting as an expansion bus. Scalability of connections between the high speed half-bridge circuits increases efficiency of data transfer.

(6) CONCISE STATEMENT OF THE ISSUES PRESENTED FOR REVIEW

(A) Whether claims 1-3, 6, 8, 10-12, 15, 17, 19-21, 24 and 26 are obvious under 35 U.S.C. §103(a) over U.S. Patent No. 6,662,254 to Tal et al. ("Tal").

(B) Whether claims 5, 7, 14, 16, 23 and 25 are obvious under 35 U.S.C. §103(a) over Tal in view of old and well-known prior art ("OWKPA").

(C) Whether claims 1-3, 6, 8, 10-12, 15, 17, 19-21, 24 and 26 are obvious under 35 U.S.C. §103(a) over U.S. Patent No. 6,606,678 to Nakamura ("Nakamura").

(D) Whether claims 5, 7, 14, 16, 23 and 25 are obvious under 35 U.S.C. §103(a) over Nakamura in view of old and well-known prior art ("OWKPA").

(E) Whether claims 1-3, 10-12, 14, 19-21 and 23 are obvious under 35 U.S.C. §103(a) over U.S. Patent No. 6,457,091 to Lange et al. ("Lange").

(F) Whether claims 6, 7, 15, 16, 24 and 25 are obvious under 35 U.S.C. §103(a) over Lange in view of old and well-known prior art ("OWKPA").

(7) WHETHER THE CLAIMS STAND OR FALL TOGETHER

Group I: Claims 1-3, 5-8, 19-21 and 23-26 stand or fall together because each includes the following distinctive features:

(1) a system relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are scalable depending on a bandwidth needed for a particular application;

Group II: Claims 10-12 and 14-17 stand or fall together because each includes the following distinctive features:

(1) a method relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are scalable depending on a bandwidth needed for a particular application.

(8) ARGUMENTS WITH RESPECT TO THE ISSUES PRESENTED FOR REVIEW

(A) Claims 1-3, 6, 8, 10-12, 15, 17, 19-21, 24 and 26 are not obvious under 35 U.S.C. § 103(a) over Tal.

All rejected claims 1-3, 6, 8, 10-12, 15, 17, 19-21, 24 and 26 require a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application.

The Examiner acknowledged in the Final Office Action dated June 2, 2005 that Tal fails to disclose a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 1-3, 6, 8, 10-12, 15, 17, 19-21, 24 and 26 (See Final Office Action dated June 2, 2005, page 4). However, the Examiner alleged that "it would have been obvious to one of ordinary skill in the art at the time of the invention was made to employ any particular number of duplex serial lines depending on a bandwidth requirement of a particular application, since using a particular number of duplex serial lines (depending on a bandwidth requirement for a particular application) is clearly a matter of design choice; and only involves ordinary skill in the art" (See Final Office Action dated June 2, 2005, page 4). The Applicants respectfully disagree.

Providing a plurality of data paths to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application is **NOT** a matter of design choice since providing **significant advantages** over the cited prior art. Scalability of data paths connecting a first half bridge circuit and a second half bridge circuit allows use of a reduced number of data paths in less demanding applications that provides, e.g., a power savings that is an important consideration in power sensitive applications. Moreover, scalability of data paths connecting a first half bridge circuit and a second half bridge circuit allows use of a reduced number of data paths in less demanding applications that, e.g., frees data paths for dedicated transmission of data in an opposite direction for application using bi-directional communications. The cited prior art fails to disclose or suggest scalability, much less disclose or suggest the claimed features having such benefits.

Moreover, modifying the cited prior art to arrive at the claimed features only involving ordinary skill in the art is **NOT** a test of patentability, i.e., patentability does not depend on if a modification of the prior art involves a skill beyond that of ordinary skill in the art. The test for patentability is if the cited prior art discloses the claimed features and if the claimed features are obvious in view

of the cited prior art. The Examiner acknowledges the cited prior art fails to disclose the claimed features. The claimed features are **NOT** obvious in view of the cited prior art since the cited prior art fails to disclose or suggest any need, i.e., motivation, for such a modification. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art **suggested** the desirability of the modification." In re Fritch, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992).

The Examiner in the Advisory Action dated September 20, 2005 that the Examiner maintains that CompactPCI is allegedly scalable and Field Programmable Gate Arrays are reconfigurable devices and one can create custom circuitry to meet specific needs, i.e., FPGAs are scalable. Moreover, the Examiner alleges that a serial channel provided by Lucent or Lattice Semiconductor (FPGA, ORCA family, cited in the Office Action dated June 2, 2005) is scalable.

The Examiner has not provided a single source to back up such statements that CompactPCI is scaleable and that FPGAs are scaleable. The Applicants respectfully request the Examiner provide support for such **NEW** contentions made in the Advisory Action dated September 20, 2005. Nevertheless, CompactPCI is based on the PCI. Peripheral Component Interconnect or PCI is a personal computer local bus that allows for connection of cards to a personal computer, i.e., modems, video cards, stands for that is standard equates to at least one of Applicants' claimed first bus segment and second bus segment. Thus, a PCI bus is part of a backplane that computer cards are connected to and is **NOT** a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit, much less a plurality of data paths that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 1-3, 6, 8, 10-12, 15, 17, 19-21, 24 and 26.

It is respectfully submitted that not only does this rejection fail on its face, and thus is improper, but also in light of the above comments its clear that Tal does not render obvious any of claims 1-3, 6, 8, 10-12, 15, 17, 19-21, 24 and

26. Thus, the rejection of claims 1-3, 6, 8, 10-12, 15, 17, 19-21, 24 and 26 under 35 U.S.C. § 103(a) is improper and should be reversed.

(B) Claims 5, 7, 14, 16, 23 and 25 are not obvious under 35 U.S.C. § 103(a) over Tal in view of OWKPA.

All rejected claims 5, 7, 14, 16, 23 and 25 require a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application.

As discussed above, Tal fails to disclose or suggest a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 5, 7, 14, 16, 23 and 25.

The Examiner relies on OWKPA to allegedly disclose the use of two buses having different frequencies and the use of a FPSC for a PCI half bridge. However, even modifying Tal with alleged OWKPA, i.e., the use of two buses having different frequencies and a FPSC for a PCI half bridge still fails to disclose or suggest a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 5, 7, 14, 16, 23 and 25.

It is respectfully submitted that not only does this rejection fail on its face, and thus is improper, but also in light of the above comments its clear that Tal in view of OWKPA does not render obvious any of claims 5, 7, 14, 16, 23 and 25. Thus, the rejection of claims 5, 7, 14, 16, 23 and 25 under 35 U.S.C. § 103(a) is improper and should be reversed.

(C) Claims 1-3, 6, 8, 10-12, 15, 17, 19-21, 24 and 26 are not obvious under 35 U.S.C. § 103(a) over Nakamura.

All rejected claims 1-3, 6, 8, 10-12, 15, 17, 19-21, 24 and 26 require a plurality of data paths used to connect a first half bridge circuit and a second

half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application.

The Examiner acknowledges that Nakamura fails to disclose a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 (See Final Office Action dated June 2, 2005, pages 6). However, the Examiner alleges that "it would have been obvious to one of ordinary skill in the art at the time of the invention was made to employ any particular number of duplex serial lines depending on a bandwidth requirement of a particular application, since using a particular number of duplex serial lines (depending on a bandwidth requirement for a particular application) is clearly a matter of design choice; and only involves ordinary skill in the art" (See Final Office Action dated June 2, 2005, page 7). The Applicants respectfully disagree.

As discussed above, providing a plurality of data paths to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application is **NOT** a matter of design choice since providing **significant advantages** over the cited prior art. Scalability of data paths connecting a first half bridge circuit and a second half bridge circuit allows use of a reduced number of data paths in less demanding applications that provides, e.g., a power savings that is an important consideration in battery driven circuits. Moreover, scalability of data paths connecting a first half bridge circuit and a second half bridge circuit allows use of a reduced number of data paths in less demanding applications that, e.g., frees data paths for dedicated transmission of data in an opposite direction for application using bi-directional communications. The cited prior art fails to disclose or suggest scalability, much less disclose or suggest the claimed features having such benefits.

Moreover as discussed above, modifying the cited prior art to arrive at the claimed features only involving ordinary skill in the art is NOT a test of patentability, i.e., patentability does not depend on if a modification of the prior art

involves a skill beyond that of ordinary skill in the art. The test for patentability is if the cited prior art discloses the claimed features and if the claimed features are obvious in view of the cited prior art. The Examiner acknowledges the cited prior art fails to disclose the claimed features. The claimed features are NOT obvious in view of the cited prior art since the cited prior art fails to disclose or suggest any need, i.e., motivation, for such a modification. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992).

Nakamura fails to disclose or suggest a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 1-3, 6, 8, 10-12, 15, 17, 19-21, 24 and 26.

It is respectfully submitted that not only does this rejection fail on its face, and thus is improper, but also in light of the above comments its clear that Nakamura does not render obvious any of claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26. Thus, the rejection of claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 under 35 U.S.C. § 103(a) is improper and should be reversed.

(D) Claims 5, 7, 14, 16, 23 and 25 are not obvious under 35 U.S.C. § 103(a) over Tal in view of OWKPA.

All rejected claims 5, 7, 14, 16, 23 and 25 require a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application.

As discussed above, Nakamura fails to disclose or suggest a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 5, 7, 14, 16, 23 and 25.

The Examiner relies on OWKPA to allegedly disclose the use of two buses having different frequencies and the use of a FPSC for a PCI half bridge. However, even modifying Tal with alleged OWKPA, i.e., the use of two

buses having different frequencies and a FPSC for a PCI half bridge still fails to disclose or suggest a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 5, 7, 14, 16, 23 and 25.

It is respectfully submitted that not only does this rejection fail on its face, and thus is improper, but also in light of the above comments its clear that Nakamura in view of OWKPA does not render obvious any of claims 5, 7, 14, 16, 23 and 25. Thus, the rejection of claims 5, 7, 14, 16, 23 and 25 under 35 U.S.C. § 103(a) is improper and should be reversed.

(E) Claims 1-3, 10-12, 14, 19-21 and 23 are not obvious under 35 U.S.C. § 103(a) over Lange.

All rejected claims 1-3, 10-12, 14, 19-21 and 23 require a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application.

The Examiner acknowledges that Lange fails to disclose a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 1-3, 10-12, 14, 19-21 and 23 (See Final Office Action dated June 2, 2005, pages 9). However, the Examiner alleges that "it would have been obvious to one of ordinary skill in the art at the time of the invention was made to employ any particular number of duplex serial lines depending on a bandwidth requirement of a particular application, since using a particular number of duplex serial lines (depending on a bandwidth requirement for a particular application) is clearly a matter of design choice; and only involves ordinary skill in the art" (See Final Office Action dated June 2, 2005, page 9). The Applicants respectfully disagree.

As discussed above, providing a plurality of data paths to connect a first half bridge circuit and a second half bridge circuit that are **scalable**

depending on a bandwidth needed for a particular application is **NOT** a matter of design choice since providing **significant advantages** over the cited prior art. Scalability of data paths connecting a first half bridge circuit and a second half bridge circuit allows use of a reduced number of data paths in less demanding applications that provides, e.g., a power savings that is an important consideration in battery driven circuits. Moreover, scalability of data paths connecting a first half bridge circuit and a second half bridge circuit allows use of a reduced number of data paths in less demanding applications that, e.g., frees data paths for dedicated transmission of data in an opposite direction for application using bi-directional communications. The cited prior art fails to disclose or suggest scalability, much less disclose or suggest the claimed features having such benefits.

Moreover as discussed above, modifying the cited prior art to arrive at the claimed features only involving ordinary skill in the art is **NOT** a test of patentability, i.e., patentability does not depend on if a modification of the prior art involves a skill beyond that of ordinary skill in the art. The test for patentability is if the cited prior art discloses the claimed features and if the claimed features are obvious in view of the cited prior art. The Examiner acknowledges the cited prior art fails to disclose the claimed features. The claimed features are **NOT** obvious in view of the cited prior art since the cited prior art fails to disclose or suggest any need, i.e., motivation, for such a modification. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992).

Lange fails to disclose or suggest a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 1-3, 10-12, 14, 19-21 and 23.

It is respectfully submitted that not only does this rejection fail on its face, and thus is improper, but also in light of the above comments its clear that Lange does not render obvious any of claims 1-3, 10-12, 14, 19-21 and 23.

Thus, the rejection of claims 1-3, 10-12, 14, 19-21 and 23 under 35 U.S.C. § 103(a) is improper and should be reversed.

(F) Claims 6, 7, 15, 16, 24 and 25 are not obvious under 35 U.S.C. § 103(a) over Lange in view of OWKPA.

All rejected claims 6, 7, 15, 16, 24 and 25 require a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application.

As discussed above, Lange fails to disclose or suggest a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 6, 7, 15, 16, 24 and 25.

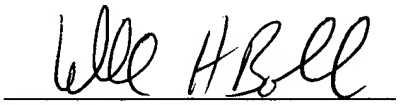
The Examiner relies on OWKPA to allegedly disclose the use of two buses having the same frequencies and the use of a FPSC for a PCI half bridge. However, even modifying Tal with alleged OWKPA, i.e., the use of two buses having the same frequencies and a FPSC for a PCI half bridge still fails to disclose or suggest a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are **scalable** depending on a bandwidth needed for a particular application, as recited by claims 6, 7, 15, 16, 24 and 25.

It is respectfully submitted that not only does this rejection fail on its face, and thus is improper, but also in light of the above comments its clear that Lange in view of OWKPA does not render obvious any of claims 6, 7, 15, 16, 24 and 25. Thus, the rejection of claims 6, 7, 15, 16, 24 and 25 under 35 U.S.C. § 103(a) is improper and should be reversed.

CONCLUSION

For all the reasons set forth above, the rejections of claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 are improper and should be reversed. The Applicants therefore respectfully request that this Appeal be granted and that the rejections of the claims be reversed.

Respectfully submitted,



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APPENDIX

CLAIMS INVOLVED IN THE APPEAL

1. A system for interconnecting two or more computer bus architectures, comprising:

a first bus segment to transmit data information;

a first half bridge circuit to connect said first bus segment;

a second bus segment to transmit data information;

a second half bridge circuit to connect said first half bridge circuit, said second half bridge circuit to transfer data information between said first bus segment and said second bus segment;

a plurality of data paths to connect said first half bridge circuit and said second half bridge circuit;

wherein said plurality of data paths to connect said first half bridge circuit and said second half bridge circuit are scalable to correspond to a bandwidth needed for a particular application.

2. The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said first bus segment is a PCI architecture bus.

3. The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said second bus segment is a PCI architecture bus.

4. (canceled)

5. The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said first bus segment operates at a different bus frequency than a bus frequency of said second bus segment.

6. The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said first bus segment operates at a substantially same bus frequency as a bus frequency of said second bus segment.

7. The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

at least one of said first half bridge circuit and said second half bridge circuit are field programmable.

8. The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said first half bridge circuit and said second half bridge circuit recover a clock signal from, respectively said first bus segment and said second bus segment.

9. (canceled)

10. A method of interconnecting two or more computer bus architectures comprising:

connecting a first half bridge circuit to a first bus segment;

connecting a second half bridge circuit to a second bus segment;

connecting said first bus segment to said second bus segment through a plurality of data paths connecting said first half bridge and said second half bridge; and

transmitting data information from said first bus segment to said second bus segment over at least one of said plurality of data paths;

wherein said plurality of data paths to connect said first half bridge circuit and said second half bridge circuit are scalable to correspond to a bandwidth needed for a particular application.

11. A method for interconnecting two or more computer bus architectures according to claim 10, wherein:

said step of transmitting data transmits data over a SCSI architecture bus.

12. A method for interconnecting two or more computer bus architectures according to claim 10, wherein:

said step of transmitting data transmits data over a PCI architecture bus.

13. (canceled)

14. A method for interconnecting two or more computer bus architectures according to claim 10, wherein:

operation of a bus frequency of said first bus segment is different than a bus frequency of said second bus segment.

15. A method for interconnecting two or more computer bus architectures according to claim 10, wherein:

operation of a bus frequency of said first bus segment is substantially the same as a bus frequency of said second bus segment.

16. A method for interconnecting two or more computer bus architectures according to claim 10, further comprising:

field programming at least one of said first half bridge circuit and said second half bridge circuit.

17. A method for interconnecting two or more computer bus architectures according to claim 10, further comprising:

recovering a clock signal for said first half bridge circuit and said second half bridge circuit from their respectively connected said first bus segment and said second bus segment.

18. (canceled)

19. A system for interconnecting two or more computer bus architectures comprising:

a first half bridge circuit means connected to a first bus segment means;

a second half bridge circuit means connected to a second bus segment means; and

a plurality of data paths means to connect said first half bridge circuit means and said second half bridge circuit means;

wherein information is passed between said first bus segment means and said second bus segment means over said first half bridge circuit means and said second half bridge circuit means; and

wherein said plurality of data paths means are scalable to correspond to a bandwidth needed for a particular application.

20. The system for interconnecting two or more computer bus architectures according to claim 19, wherein:

said first bus segment is a PCI architecture bus.

21. The system for interconnecting two or more computer bus architectures according to claim 19, wherein:

said second bus segment means is a PCI architecture bus.

22. (canceled)

23. The system for interconnecting two or more computer bus architectures according to claim 19, wherein:

said first bus segment means bus frequency is different than said second bus segment means bus frequency.

24. The system for interconnecting two or more computer bus architectures according to claim 19, wherein:

said first bus segment means bus frequency is the same as said second bus segment means bus frequency.

25. The system for interconnecting two or more computer bus architectures according to claim 19, further comprising:

at least one of said first half bridge circuit means and said second half bridge circuit means are field programmable.

26. The system for interconnecting two or more computer bus architectures according to claim 19, further comprising:

said first half bridge circuit means and said second half bridge circuit means recover a clock signal from their respectively connected said first bus segment means and said second bus segment means.

27. (canceled)